

Preliminary W25P010A



32K × 32 BURST PIPELINED HIGH-SPEED CMOS STATIC RAM

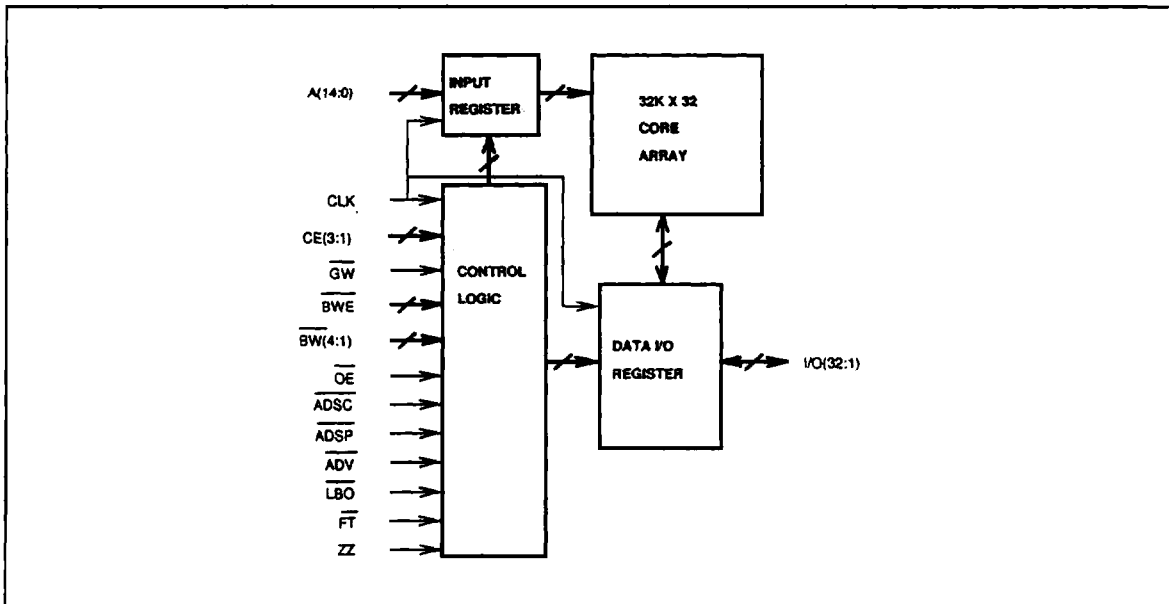
GENERAL DESCRIPTION

The W25P010A is a high-speed, synchronous-burst-pipelined, low-power CMOS static RAM organized as 32,768 × 32 bits that operates on a single 3.3-volt power supply. A built-in two-bit burst address counter supports both i486™/Pentium™ burst mode and linear burst mode. The mode to be executed is controlled by the $\overline{\text{LBO}}$ pin. Pipelining or non-pipelining of the data outputs is controlled by the $\overline{\text{FT}}$ pin. A snooze mode can reduce power dissipation.

FEATURES

- Synchronous operation
- High-speed access time: 7/8/10 nS (max.)
- Single +3.3V power supply
- Individual byte write capability
- 3.3V LVTTTL compatible I/O
- Clock-controlled and registered input
- Asynchronous output enable
- Pipelined/non-pipelined data output capability
- Supports snooze mode (low-power state)
- Internal burst counter supports Intel burst mode & linear burst mode
- Available in 100-pin QFP/TQFP packages

BLOCK DIAGRAM



WINBOND
WINDS013



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
A0-A14	Input, Synchronous	Host Address
I/O1-I/O32	I/ O, Synchronous	Data Inputs/ Outputs
CLK	Input, Clock	Processor Host Bus Clock
$\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$	Input, Synchronous	Chip Enables
\overline{GW}	Input, Synchronous	Global Write
\overline{BWE}	Input, Synchronous	Byte Write Enable from Cache Controller
$\overline{BW1}$ - $\overline{BW4}$	Input, Synchronous	Host Bus Byte Enables Used with \overline{BWE}
\overline{OE}	Input, Asynchronous	Output Enable Input
\overline{ADV}	Input, Synchronous	Internal Burst Address Counter Advance
\overline{ADSC}	Input, Synchronous	Address Status from CPU
\overline{ADSP}	Input, Synchronous	Address Status from Chip Set
ZZ	Input, Asynchronous	Snooze Pin for Low-power State, Internal Pull Low
\overline{FT}	Input, Static	Flow-through for Non-pipelined Mode When Connected to VSSQ, Internal Pull High
\overline{LBO}	Input, Static	Lower Address Burst Order for Linear Burst Mode When Connected to VSSQ, Internal Pull High
VDDQ		I/O Power Supply
VSSQ		I/O Ground
VDD		Power Supply
VSS		Ground



TRUTH TABLE

CYCLE	ADDRESS USED	$\overline{CS1}$	CE2	$\overline{CS3}$	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{OE}	DATA	WRITE*
Unselected	No	1	X	X	X	0	X	X	Hi-Z	X
Unselected	No	0	X	1	0	X	X	X	Hi-Z	X
Unselected	No	0	0	X	0	X	X	X	Hi-Z	X
Unselected	No	0	X	1	1	0	X	X	Hi-Z	X
Unselected	No	0	0	X	1	0	X	X	Hi-Z	X
Begin Read	External	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	X	X	X	1	1	0	0	D-Out	Read
Continue Read	Next	1	X	X	X	1	0	1	Hi-Z	Read
Continue Read	Next	1	X	X	X	1	0	0	D-Out	Read
Suspend Read	Current	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	X	X	X	1	1	1	0	D-Out	Read
Suspend Read	Current	1	X	X	X	1	1	1	Hi-Z	Read
Suspend Read	Current	1	X	X	X	1	1	0	D-Out	Read
Begin Write	Current	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	1	X	X	X	1	1	X	Hi-Z	Write
Begin Write	External	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	1	X	X	X	1	0	X	Hi-Z	Write
Suspend Write	Current	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	1	X	X	X	1	1	X	Hi-Z	Write

Notes:

1. For a detailed definition of read/write, see the Write Table below.
2. An "X" means "don't care," "1" means logic high, and "0" means logic low.
3. The \overline{OE} pin enables the data output but is not synchronous with the clock. All signals of the SRAM are sampled synchronous to the bus clock except for the \overline{OE} pin.
4. On a write cycle that follows a read cycle, \overline{OE} must be inactive prior to the start of write cycle to allow write data to setup the SRAM. \overline{OE} must also disable the output buffer prior to the finish of a write cycle to ensure the SRAM data hold timing are met.



FUNCTIONAL DESCRIPTION

The W25P010A is a synchronous burst and pipelined, which can be also switched to non-pipelined, SRAM designed for use in high-end personal computers. It supports two burst address sequences for Intel™ systems and linear mode, which can be controlled by the \overline{LBO} pin. The burst cycles are initiated by \overline{ADSP} or \overline{ADSC} and the burst counter increases whenever \overline{ADV} is sampled low.

Burst Address Sequence

	INTEL SYSTEM ($\overline{LBO} = V_{DDQ}$)				LINEAR MODE ($\overline{LBO} = V_{SSQ}$)			
	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]
External Start Address	00	01	10	11	00	01	10	11
Second Address	01	00	11	10	01	10	11	00
Third Address	10	11	00	01	10	11	00	01
Fourth Address	11	10	01	00	11	00	01	10

The device supports different kinds of write mode operations. The \overline{BWE} and $\overline{BW}[4:1]$ support individual byte writes. The $\overline{BE}[7:0]$ signals can be directly connected to the SRAM $\overline{BW}[4:1]$. The \overline{GW} signal is used to override the byte enable signals and allows the cache controller to write all bytes to the SRAM, no matter what the byte write enable signals are. The various write modes are indicated in the Write Table below. Note that in pipelined mode, the byte write enable signals are not latched by the SRAM with addresses but with data. In pipelined mode, the cache controller must ensure the SRAM latches both data and valid byte enable signals from the processor.

WRITE TABLE

READ/WRITE FUNCTION	\overline{GW}	\overline{BWE}	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write byte 1 I/O1-I/O8	1	0	1	1	1	0
Write byte 2 I/O9-I/O16	1	0	1	1	0	1
Write byte 2, byte 1	1	0	1	1	0	0
Write byte 3 I/O17-I/O24	1	0	1	0	1	1
Write byte 3, byte 1	1	0	1	0	1	0
Write byte 3, byte 2	1	0	1	0	0	1
Write byte 3, byte 2, byte 1	1	0	1	0	0	0
Write byte 4 I/O25-I/O32	1	0	0	1	1	1
Write byte 4, byte 1	1	0	0	1	1	0



Write table, continued

READ/WRITE FUNCTION	\overline{GW}	\overline{BWE}	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Write byte 4, byte 2	1	0	0	1	0	1
Write byte 4, byte 2, byte 1	1	0	0	1	0	0
Write byte 4, byte 3	1	0	0	0	1	1
Write byte 4, byte 3, byte 1	1	0	0	0	1	0
Write byte 4, byte 3, byte 2	1	0	0	0	0	1
Write all bytes I/O-I/O32	1	0	0	0	0	0
Write all bytes I/O1-I/O32	0	X	X	X	X	X

The ZZ state is a low-power state in which the device consumes less power than in the unselected mode. Enabling the ZZ pin for a fixed period of time will force the SRAM into the ZZ state. Pulling the ZZ pin low for a set period of time will wake up the SRAM again. While the SRAM is in ZZ mode, data retention is guaranteed, but the chip will not monitor any input signal except for the ZZ pin. In the unselected mode, on the other hand, all the input signals are monitored.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Core Supply Voltage to Vss	-0.5 to 4.6	V
I/O Supply Voltage to Vss	-0.5 to 4.6	V
Input/Output to Vss Potential	VSSQ-0.5 to VDDQ+0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to 150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

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OPERATING CHARACTERISTICS

(V_{DD} = 3.15V to 3.6V, V_{SS} = 0V, T_a = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-	+2.0	-	V _{DD} +0.3	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , and data I/O pins in high-Z state defined in truth table	-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA	2.4	-	-	V
Operating Current	I _{DD}	T _{CYC} ≥ Min. , I/O = 0 mA	-	-	200	mA
Standby Current	I _{SB}	Unselected mode defined in truth table, V _{IN} = V _{IH} /V _{IL} T _{CYC} ≥ Min.	-	-	80	mA
ZZ Mode Current	I _{ZZ}	ZZ mode, T _{CYC} ≥ Min.	-	-	5	mA

Note: Typical characteristics are measured at V_{DD} = 3.3V, T_a = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_a = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

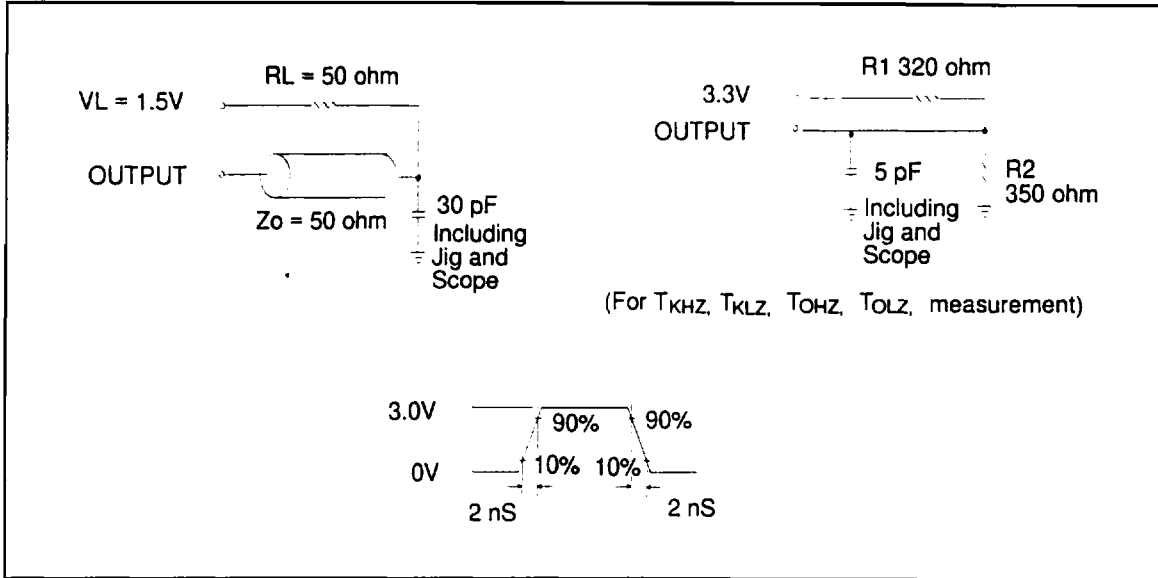
Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	2 nS
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 30 pF, I _{OH} /I _{OL} = -4 mA/8 mA



AC TEST LOADS AND WAVEFORM



AC TIMING CHARACTERISTICS

(VDD = 3.15V to 3.6V, VSS = 0V, Ta = 0 to 70° C, All timings measured in pipelined mode)

PARAMETER	SYM.	W25P010A-7		W25P010A-8		W25P010A-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Add. Setup Time	TAS	2.5	-	2.5	-	2.5	-	nS	
Add. Hold Time	TAH	0.5	-	0.5	-	0.5	-	nS	
Write Data Setup Time	TDS	2.5	-	2.5	-	2.5	-	nS	
Write Data Hold Time	TDH	0.5	-	0.5	-	0.5	-	nS	
\overline{ADV} Setup Time	TADVS	2.5	-	2.5	-	2.5	-	nS	
\overline{ADV} Hold Time	TADVH	0.5	-	0.5	-	0.5	-	nS	
\overline{ADSP} Setup Time	TADSS	2.5	-	2.5	-	2.5	-	nS	
\overline{ADSP} Hold Time	TADSH	0.5	-	0.5	-	0.5	-	nS	
\overline{ADSC} Setup Time	TADCS	2.5	-	2.5	-	2.5	-	nS	
\overline{ADSC} Hold Time	TADCH	0.5	-	0.5	-	0.5	-	nS	
$\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ Setup Time	TCES	2.5	-	2.5	-	2.5	-	nS	
$\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ Hold Time	TCEH	0.5	-	0.5	-	0.5	-	nS	
\overline{GW} , \overline{BWE} X Setup Time	TWS	2.5	-	2.5	-	2.5	-	nS	
\overline{GW} , \overline{BWE} X Hold Time	TWH	0.5	-	0.5	-	0.5	-	nS	

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AC timing characteristics, continued

PARAMETER	SYM.	W25P010A-7		W25P010A-8		W25P010A-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock Cycle Time	TCYC	13.3	-	15	-	17	-	nS	
Clock High Pulsh Width	TKH	5	-	6	-	6	-	nS	
Clock Low Pulse Width	TKL	5	-	6	-	6	-	nS	
Clock to Output Valid	TKQ	-	7	-	8	-	10	nS	
Clock to Output High-Z	TKHZ	2	13.3	2	15	2	17	nS	1
Clock to Output Low-Z	TKLZ	0	-	0	-	0	-	nS	1
Clock to Output Invalid	TKX	2	-	2	-	2	-	nS	1
Output Enable to Output Valid	TOE	-	7	-	8	-	10	nS	
Output Enable to Output High-Z	TOHZ	-	7	-	8	-	10	nS	1
Output Enable to Output Low-Z	TOLZ	0	-	0	-	0	-	nS	1
Output Enable to Output Invalid	TOX	0	-	0	-	0	-	nS	
ZZ Standby Time	TZZS	-	100	-	100	-	100	nS	2
ZZ Recover Time	TZZR	100	-	100	-	100	-	nS	3

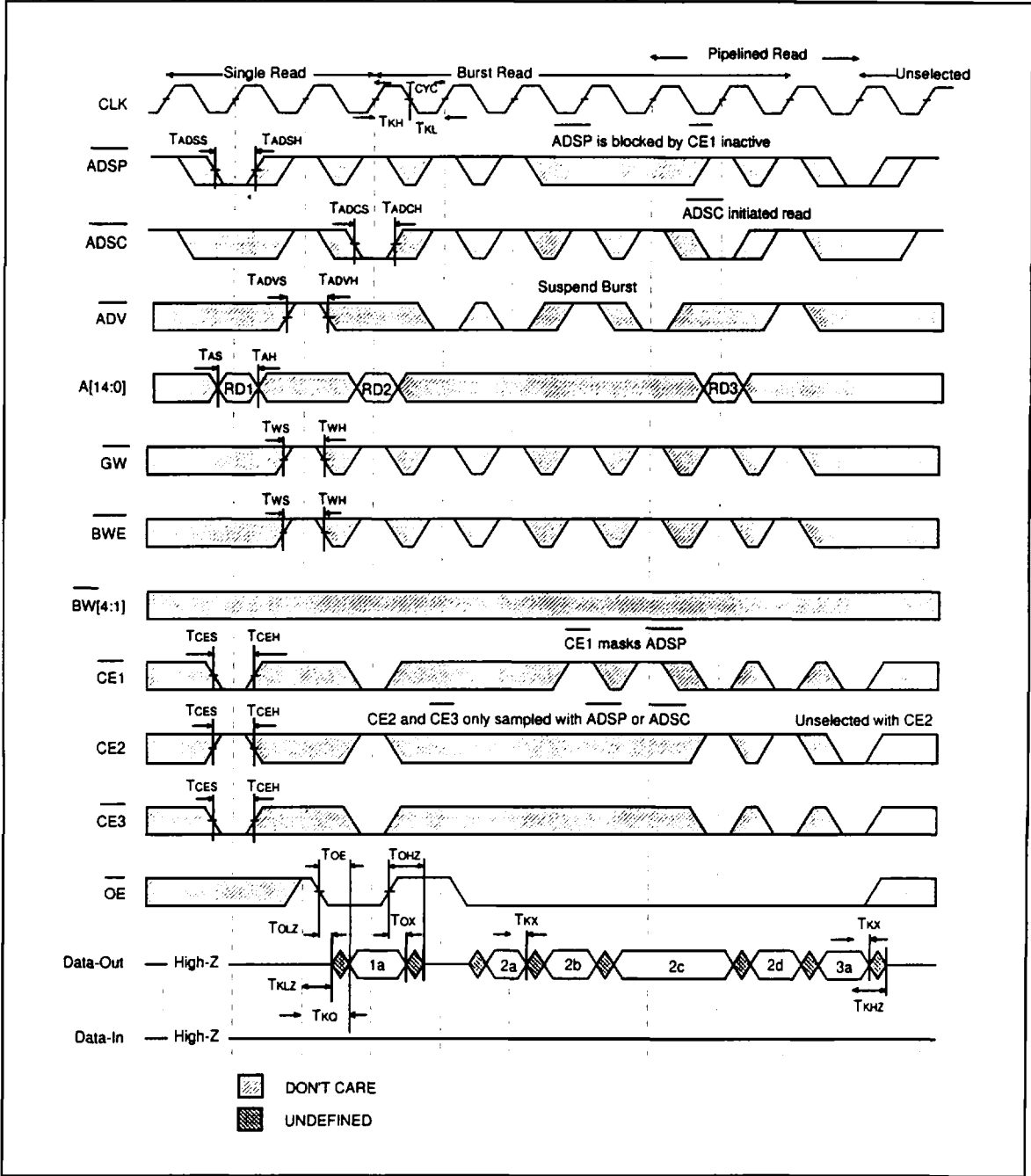
Notes:

1. These parameters are sampled but not 100% tested
2. In the ZZ mode, the SRAM will enter a low-power state. In this mode, data retention is guaranteed and the clock is active.
3. \overline{ADSC} and \overline{ADSP} should not be accessed for at least 100 nS after chip leaves ZZ mode.
4. Configuring signals \overline{LBO} and \overline{FT} are static and should not be changed during operations.



TIMING WAVEFORMS

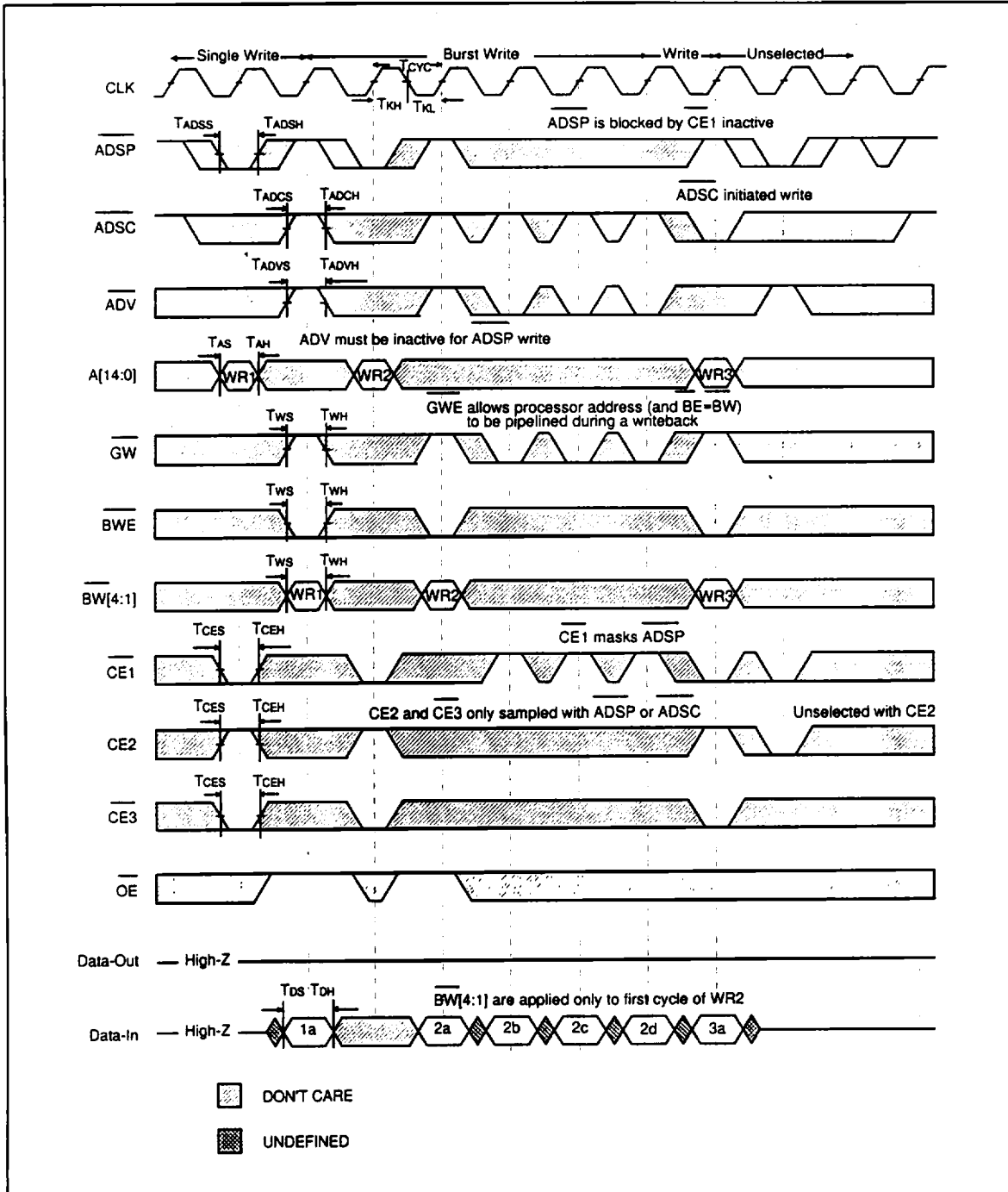
Read Cycle Timing





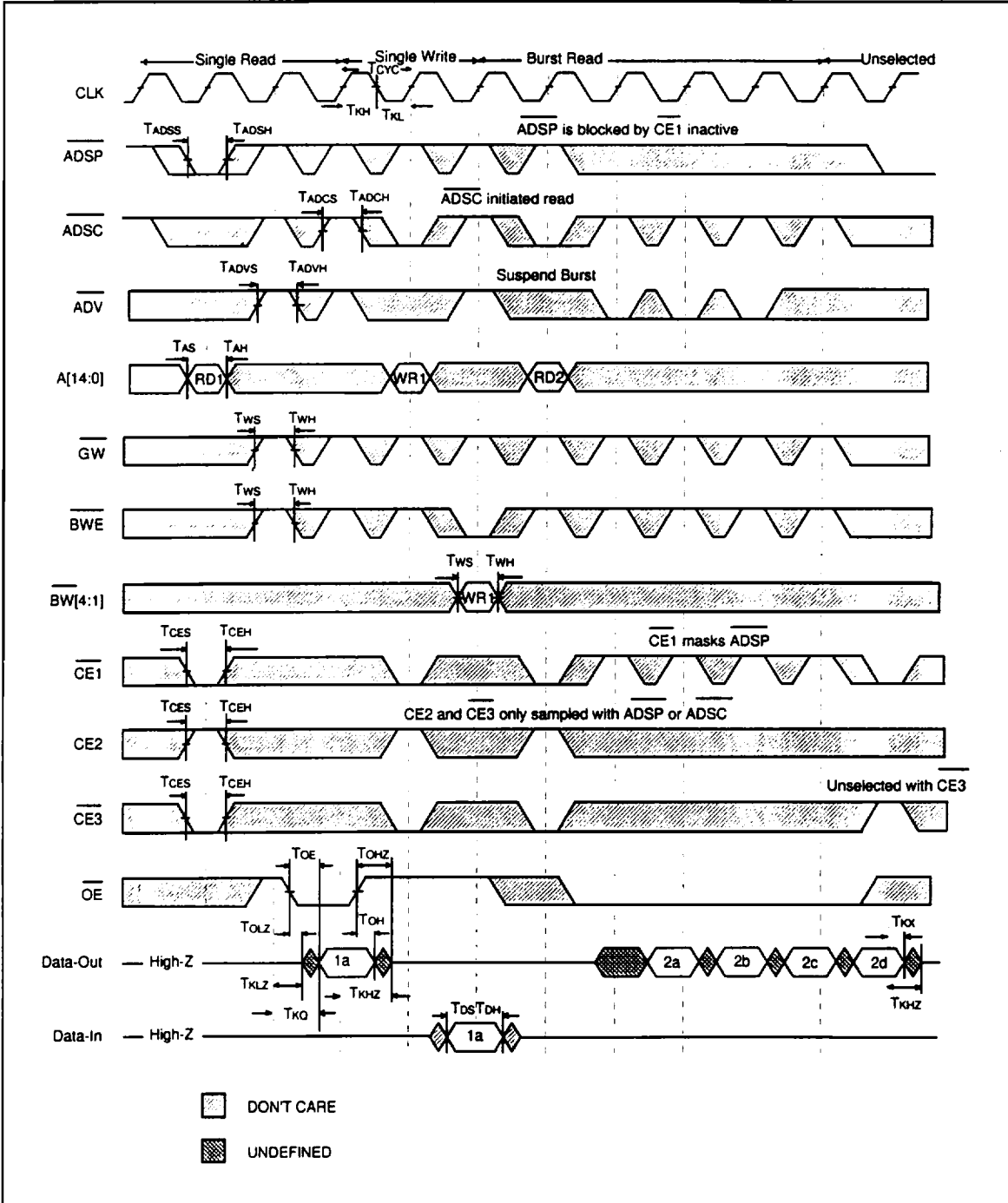
Timing waveforms, continued

Write Cycle Timing





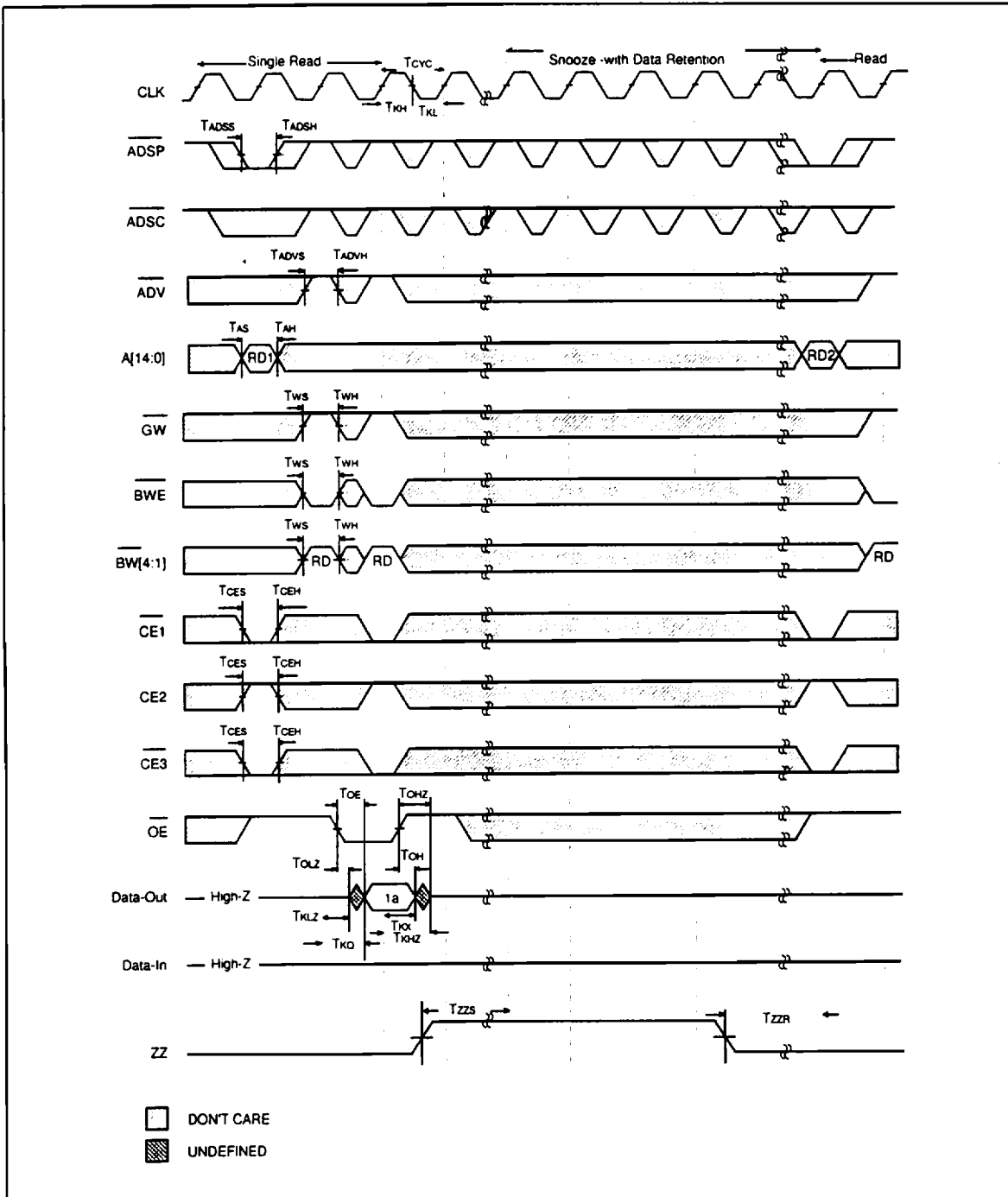
Timing waveforms, continued
Read/Write Cycle Timing





Timing waveforms, continued

ZZ and RD Timing



W25P010A



ORDERING INFORMATION

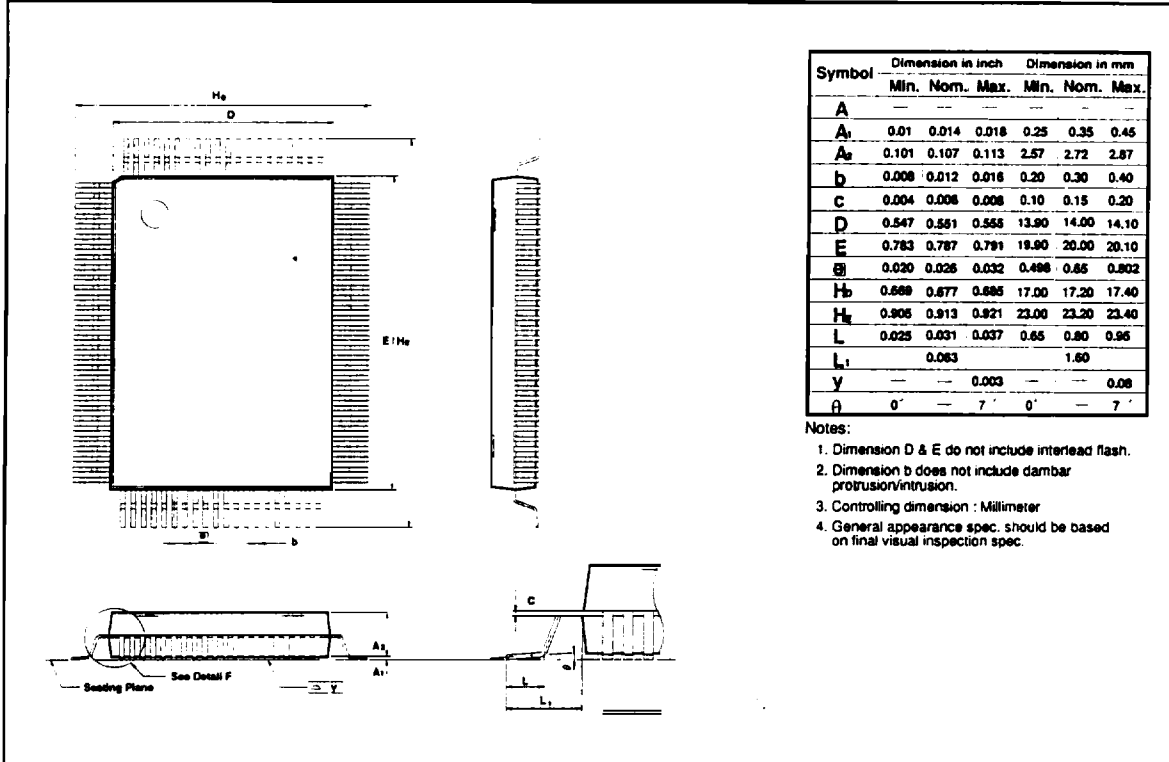
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W25P010AF-7	7	200	80	100 Lead, QFP
W25P010AF-8	8	200	80	100 Lead, QFP
W25P010AF-10	10	200	80	100 Lead, QFP
W25P010AD-7	7	200	80	100 Lead, TQFP
W25P010AD-8	8	200	80	100 Lead, TQFP
W25P010AD-10	10	200	80	100 Lead, TQFP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

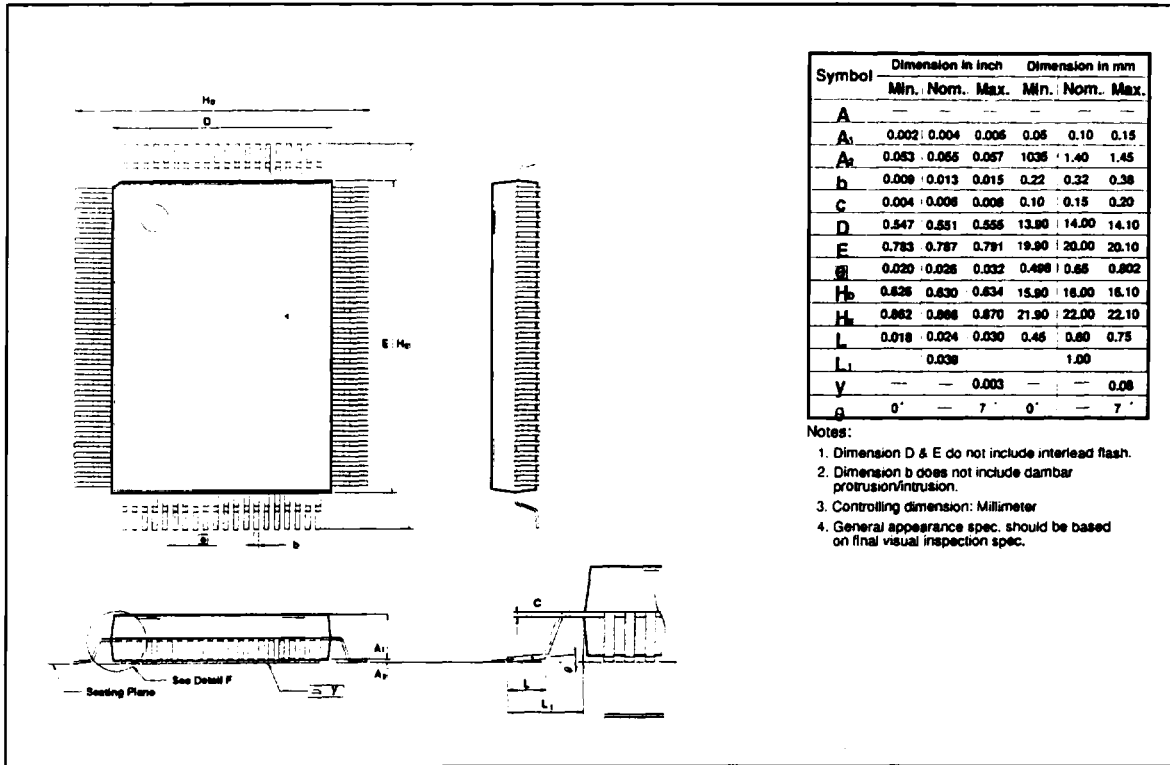
100-Lead QFP



W25P010A



100-Lead TQFP



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Note: All data and specifications are subject to change without notice.